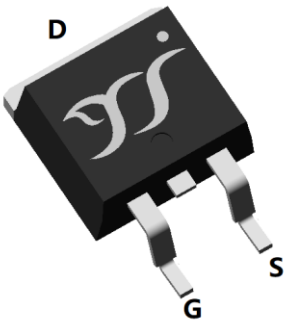
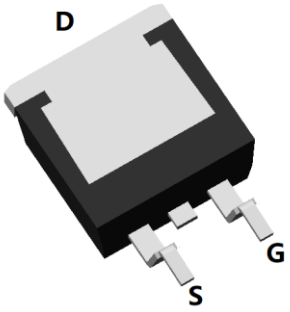
N-Channel Enhancement Mode Field Effect Transistor



Top View



Bottom View

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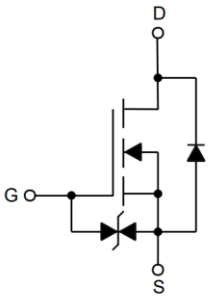


Product Summary

- V_{DS} 60V
- I_D (Silicon limited) 150A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜3.5 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜5.0 mohm
- 100% EAS Tested
- 100% ▽V_{DS} Tested
- ESD Protected up to 2.0KV(HBM)

General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Synchronous Rectification
- Battery Protection Circuit
- Motor drivers and Uninterruptible Power Supplies

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current (Silicon limited)	T_A=25℃	I_D	18	A
	T_A=100℃		11	
	T_C=25℃		150	
	T_C=100℃		95	
Pulsed Drain Current [A]		I_{DM}	450	A
Avalanche energy [B]		E_{AS}	441	mJ
Total Power Dissipation [C]	T_A=25℃	P_D	2	W
	T_A=100℃		0.8	
	Tc=25℃		147	
	Tc=100℃		59	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	t≤10S	$R_{\theta JA}$	12	15	℃/W
Thermal Resistance Junction-to-Ambient [D]	Steady-State		48	60	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.7	0.85	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJB150G06AK	F2	YJB150G06AK	800	/	8000	13“ reel

■ Electrical Characteristics (T_j=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60,V_{GS}=0V			1	μA
		V_{DS}=60,V_{GS}=0V, Tj=150℃			100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±10	μA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.7	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=20A		2.7	3.5	mΩ
		V_{GS}= 4.5V, I_D=20A		3.5	4.8	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.8	1.3	V
Maximum Body-Diode Continuous Current	I_S				150	A
Gate resistance	R_G	f= 1 MHz		2.0		Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=30V,V_{GS}=0V,f=1MHZ		4650		pF
Output Capacitance	C_{oss}			850		
Reverse Transfer Capacitance	C_{rss}			65		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=30V,I_D=25A		71		nC
Gate-Source Charge	Q_{gs}			17		
Gate-Drain Charge	Q_{gd}			10.5		
Reverse Recovery Chrage	Q_{rr}	I_F=20A, di/dt=500A/us		39.8		
Reverse Recovery Time	t_{rr}			41.6		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=30V,ID=25A R_{GEN}=2Ω		15.9		
Turn-on Rise Time	t_r			55.2		
Turn-off Delay Time	$t_{D(off)}$			57.5		
Turn-off fall Time	t_f			91.3		

A. Repetitive rating; pulse width limited by max. junction temperature.
B. V_{DD}=50V, R_G=25Ω, L=0.5mH, I_{AS}=42A.
C. Pd is based on max. junction temperature, using junction-case thermal resistance.
D. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

■ Typical Performance Characteristics

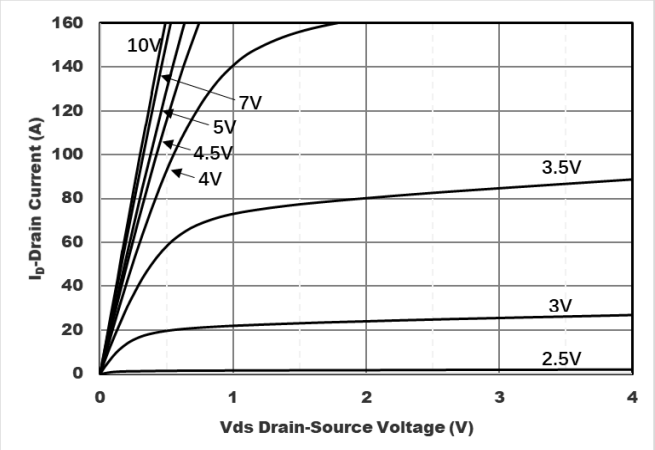


Figure1. Output Characteristics

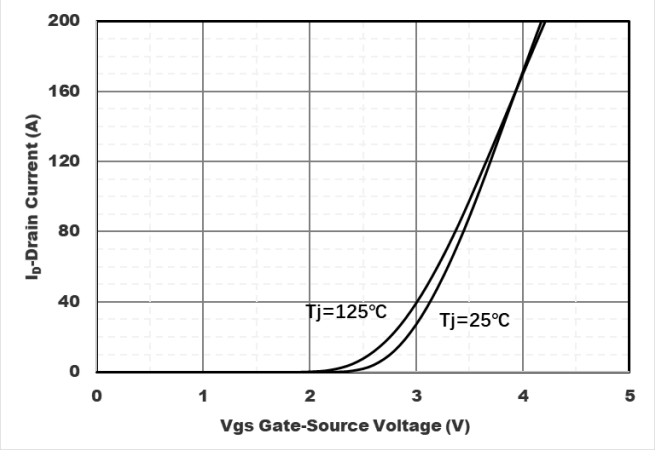


Figure2. Transfer Characteristics

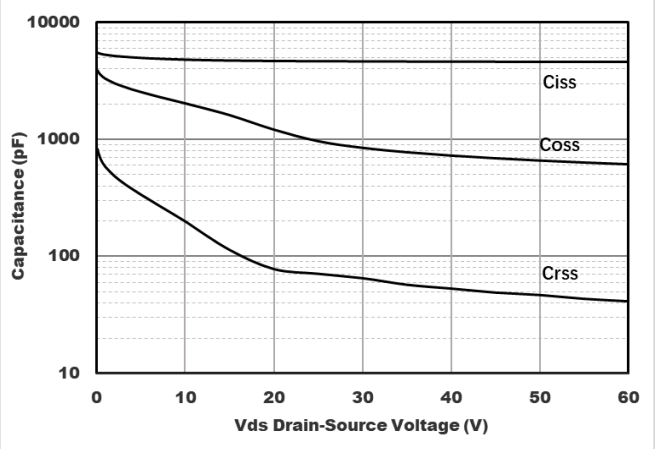


Figure3. Capacitance Characteristics

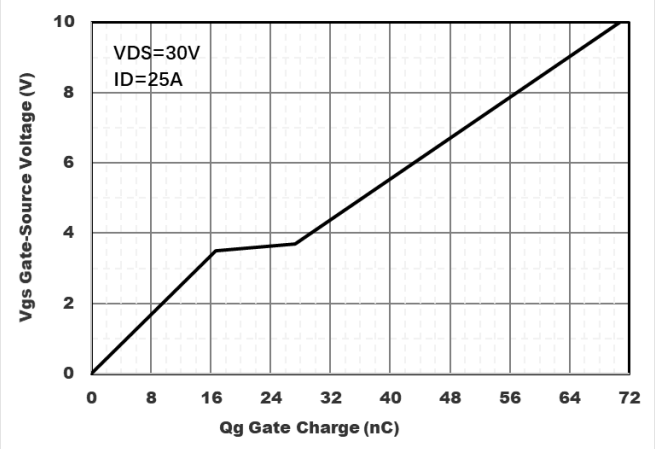


Figure4. Gate Charge

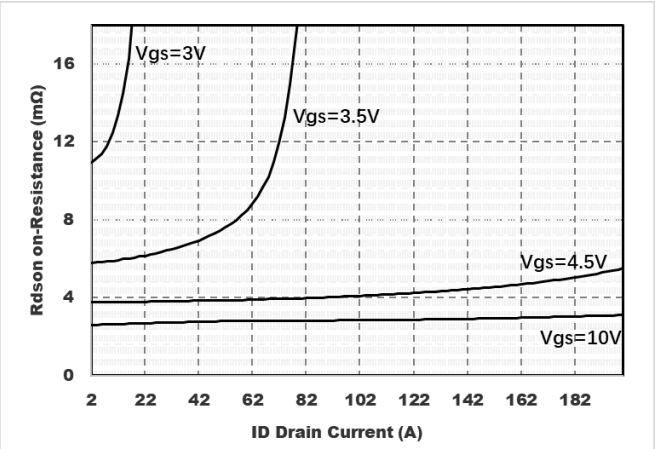


Figure5. On-Resistance vs. Drain Current and Gate Voltage

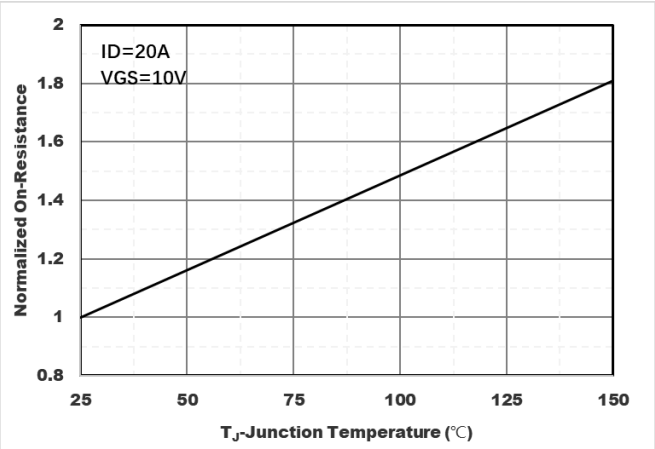


Figure6. Normalized On-Resistance

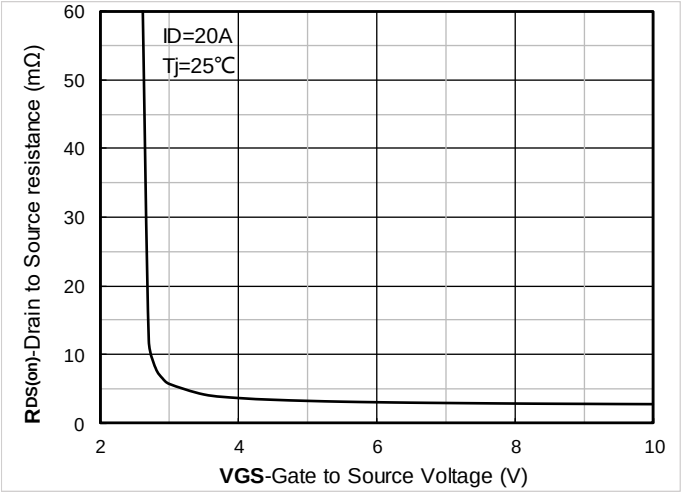


Figure 7. On-Resistance vs Gate to Source Voltage

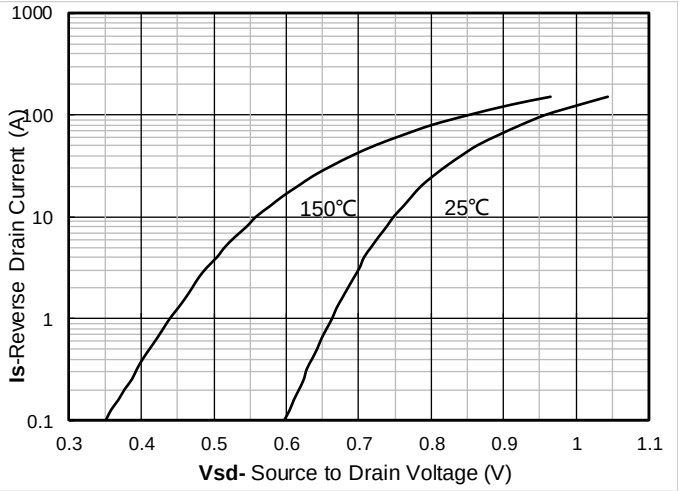


Figure 8. Forward characteristics of reverse diode

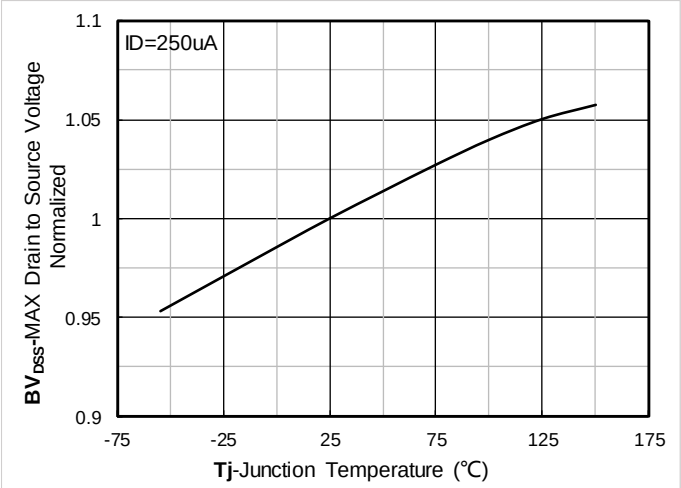


Figure 9. Normalized breakdown voltage

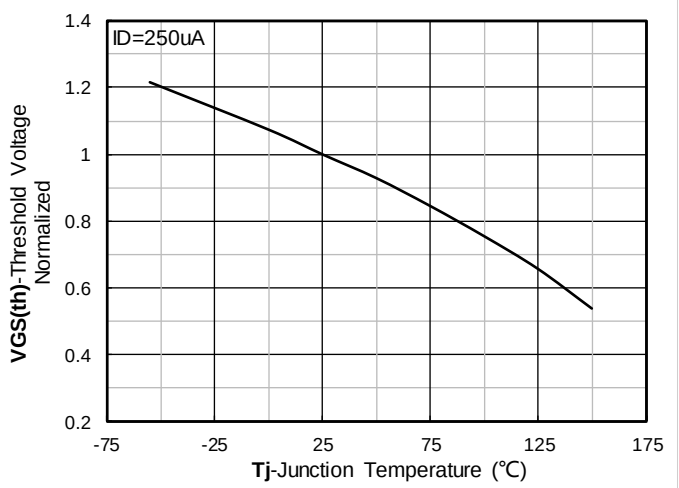


Figure 10. Normalized Threshold voltage

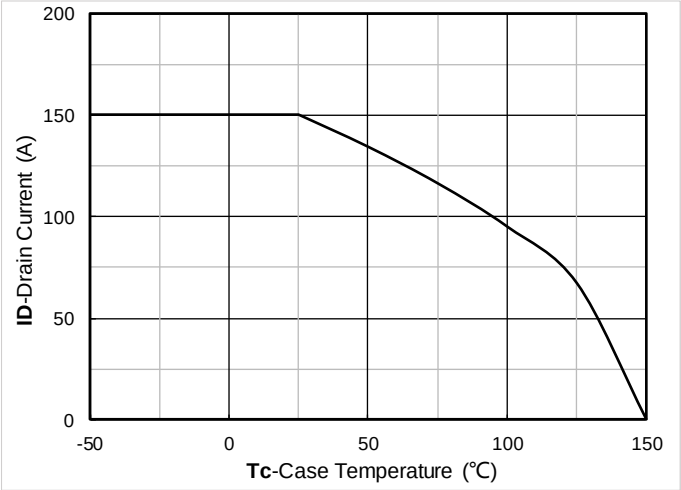


Figure 11. Current dissipation

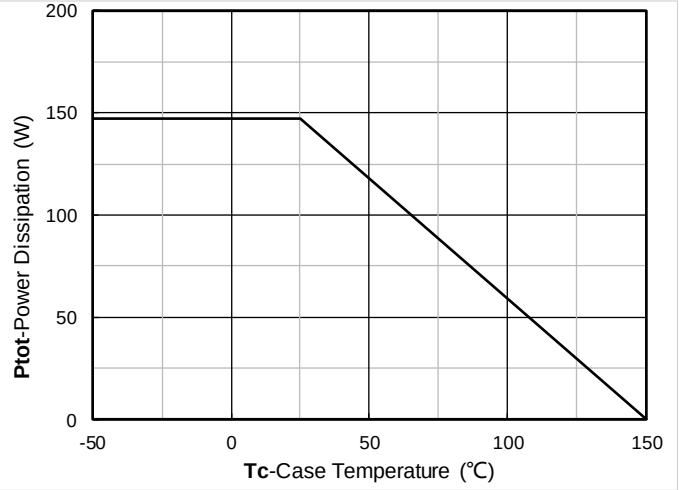


Figure 12. Power dissipation

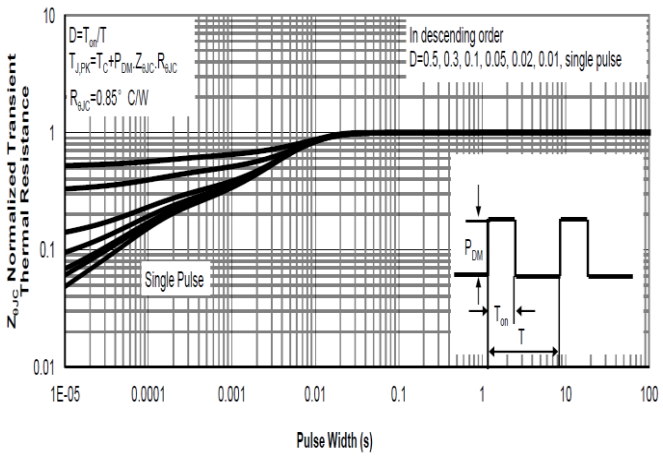


Figure13. Normalized Maximum Transient thermal impedance

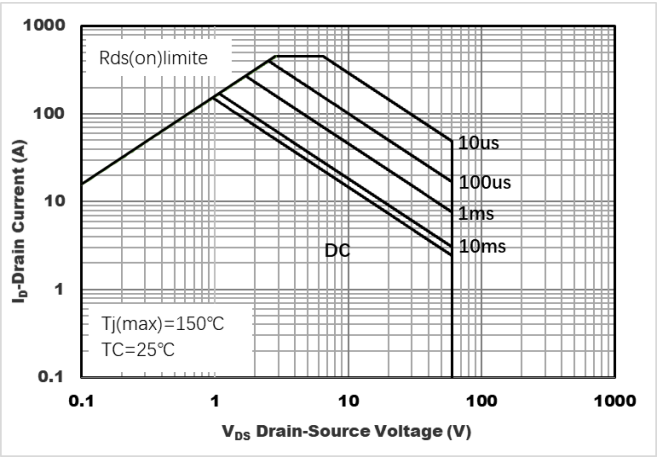
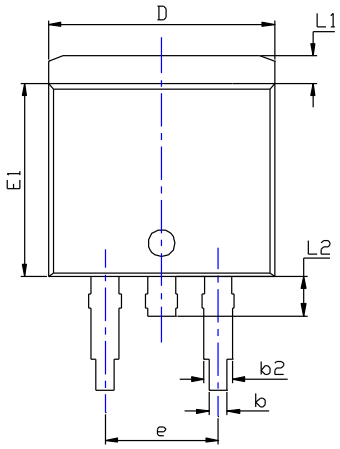
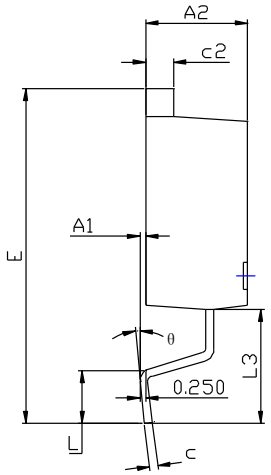


Figure14. Safe Operation Area

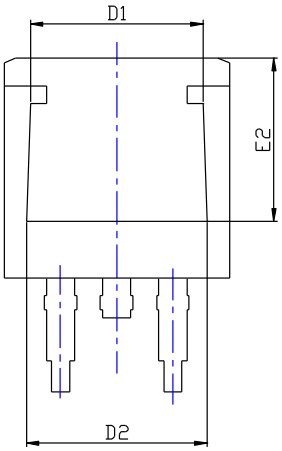
■ TO-263-HY Package information



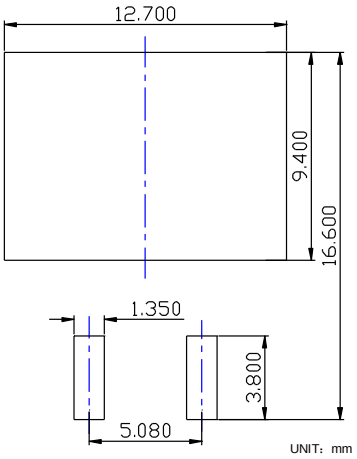
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS						
SYMBOL	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.010	0.000	---	0.250
A2	0.174	0.180	0.186	4.430	4.580	4.730
b	0.028	0.032	0.036	0.720	0.820	0.920
b2	0.046	0.050	0.054	1.180	1.280	1.380
c	0.013	0.015	0.018	0.330	0.390	0.450
c2	0.048	0.050	0.053	1.220	1.280	1.340
D	0.394	0.400	0.406	10.000	10.150	10.300
D1	0.295	0.307	0.319	7.500	7.800	8.100
D2	0.303	0.315	0.327	7.700	8.000	8.300
E	0.571	0.591	0.610	14.500	15.000	15.500
E1	0.337	0.341	0.348	8.550	8.700	8.850
E2	0.276	0.287	0.299	7.000	7.300	7.600
e	0.200BSC			5.080BSC		
L	0.070	---	0.110	1.790	---	2.790
L1	0.044	---	0.056	1.120	---	1.420
L2	0.030	---	0.070	0.770	---	1.770
L3	0.197REF			5.000REF		
θ	0°	---	8°	0°	---	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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