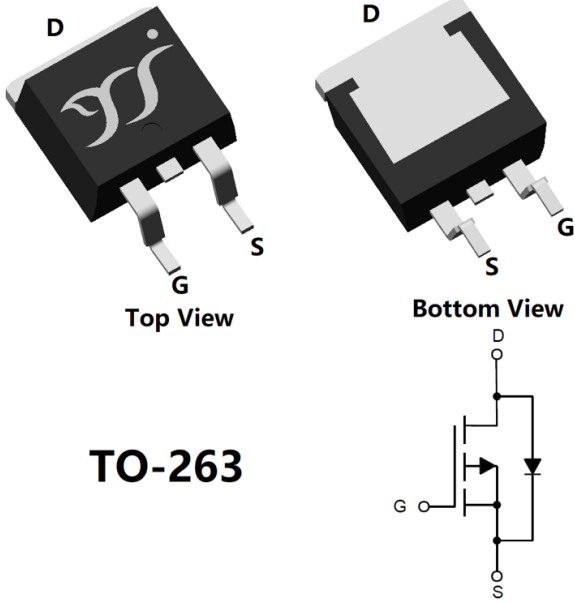


## P-Channel Enhancement Mode Field Effect Transistor



### Product Summary

- $V_{DS}$  -100V
- $I_D$  -30A
- $R_{DS(ON)}$  ( at  $V_{GS}=-10V$ ) <56 mohm
- $R_{DS(ON)}$  ( at  $V_{GS}=-4.5V$ ) <62 mohm
- 100% EAS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- DC-DC Converters
- Power management functions

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	-100	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_C=25^\circ\text{C}$	$I_D$	-30	A
	$T_C=100^\circ\text{C}$		-19.2	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	-120	A
Avalanche energy <sup>B</sup>		$E_{AS}$	162	mJ
Total Power Dissipation <sup>C</sup>	$T_C=25^\circ\text{C}$	$P_D$	125	W
	$T_C=100^\circ\text{C}$		50	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$t \leq 10\text{S}$	$R_{\theta JA}$	12	15	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State		50	60	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.8	1.0	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJB30GP10A	F2	YJB30GP10A	800	/	8000	13" reel



# YJB30GP10A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-100			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-100V, V <sub>GS</sub> =0V	T <sub>J</sub> =25°C		-1	μA
			T <sub>J</sub> =55°C		-5	
			T <sub>J</sub> =125°C		-10	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.0	-1.8	-2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-15A		42	56	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-7A		46	62	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-15A, V <sub>GS</sub> =0V			-1.3	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				-30	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-50V, V <sub>GS</sub> =0V, f=1MHZ		2100		pF
Output Capacitance	C <sub>oss</sub>			236		
Reverse Transfer Capacitance	C <sub>rss</sub>			48		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g(-10V)</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-50V, I <sub>D</sub> =-5A		40		nC
Total Gate Charge	Q <sub>g(-4.5V)</sub>			19.4		
Gate-Source Charge	Q <sub>gs</sub>			7.8		
Gate-Drain Charge	Q <sub>gd</sub>			8.6		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =-5A, di/dt=100A/us		280		nC
Reverse Recovery Time	t <sub>rr</sub>			104		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V, V <sub>DD</sub> =-50V, I <sub>DS</sub> =-5A R <sub>GEN</sub> =6Ω		13		ns
Turn-on Rise Time	t <sub>r</sub>			39		
Turn-off Delay Time	t <sub>D(off)</sub>			100.1		
Turn-off fall Time	t <sub>f</sub>			105.3		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V<sub>DD</sub>=50V, R<sub>G</sub>=25Ω, L=0.5mH.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation PDSM is based on RθJA ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



## ■ Typical Performance Characteristics

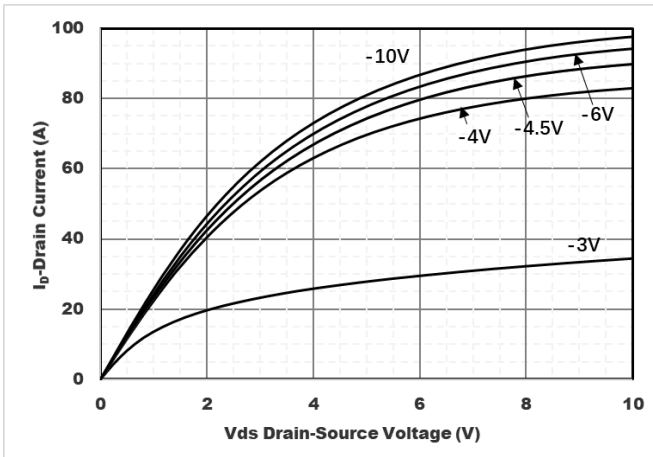


Figure1. Output Characteristics

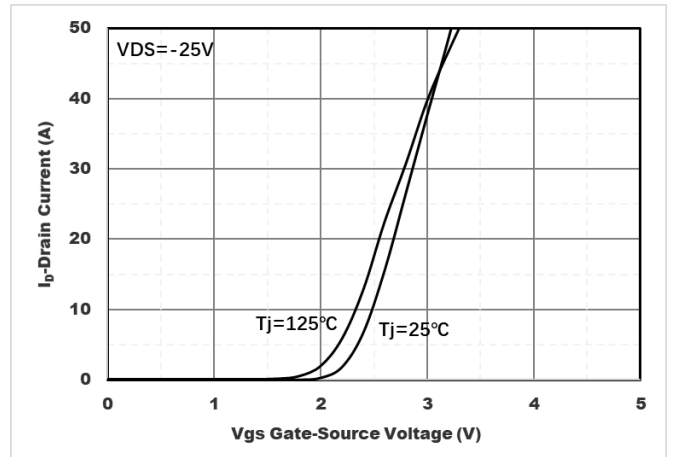


Figure2. Transfer Characteristics

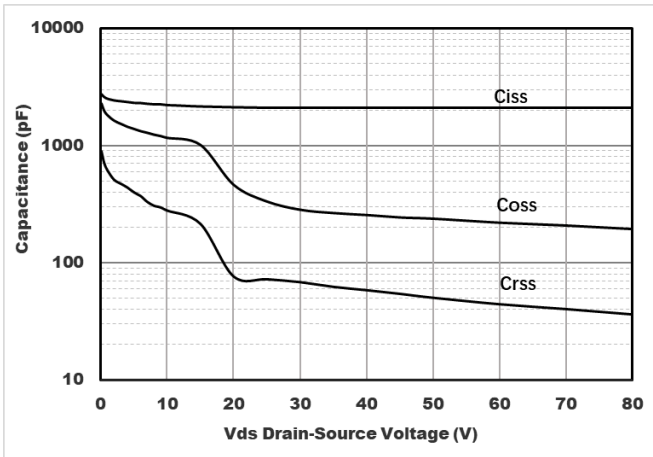


Figure3. Capacitance Characteristics

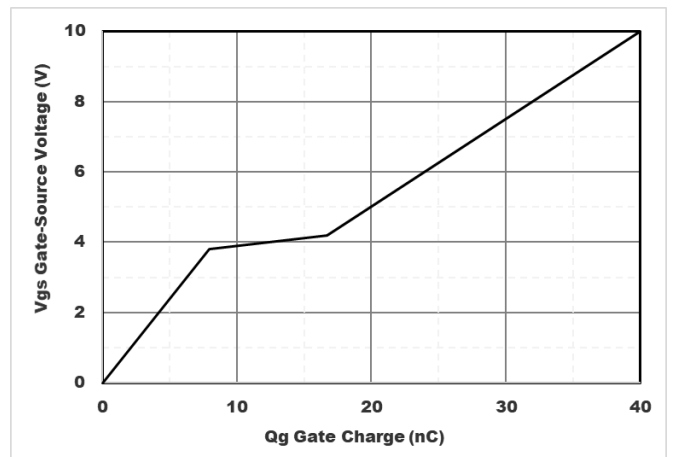


Figure4. Gate Charge

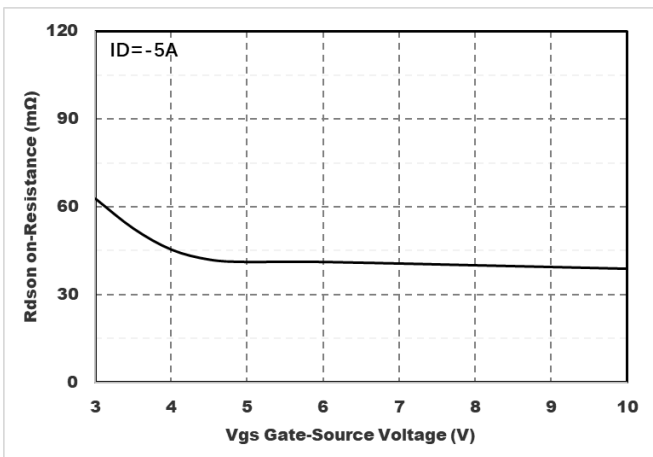


Figure5. : On-Resistance vs. Gate to Source Voltage

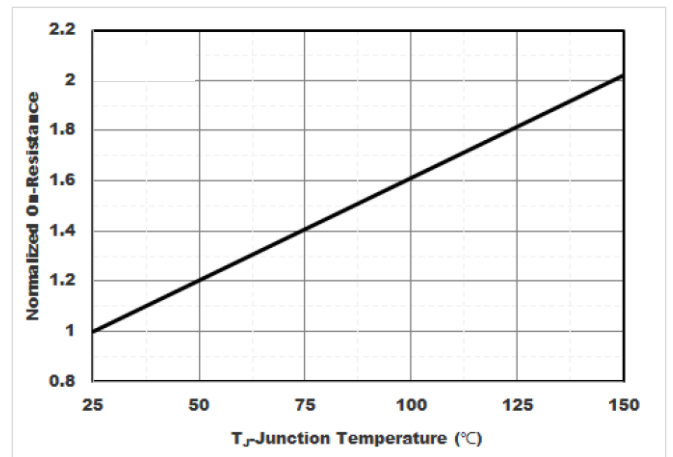


Figure6. Normalized On-Resistance



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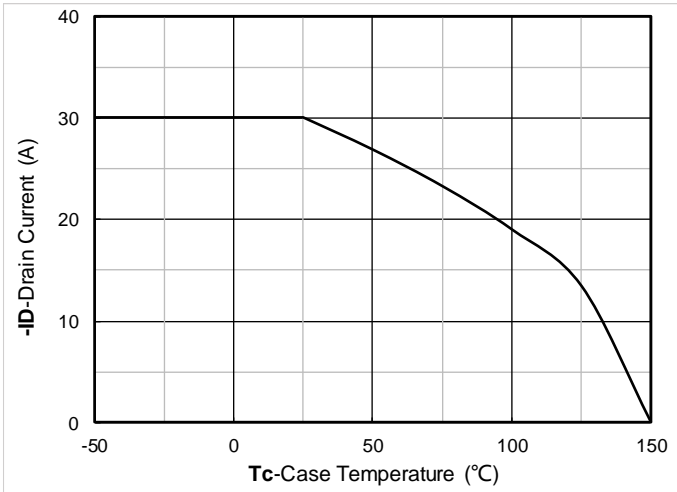


Figure7. Drain current

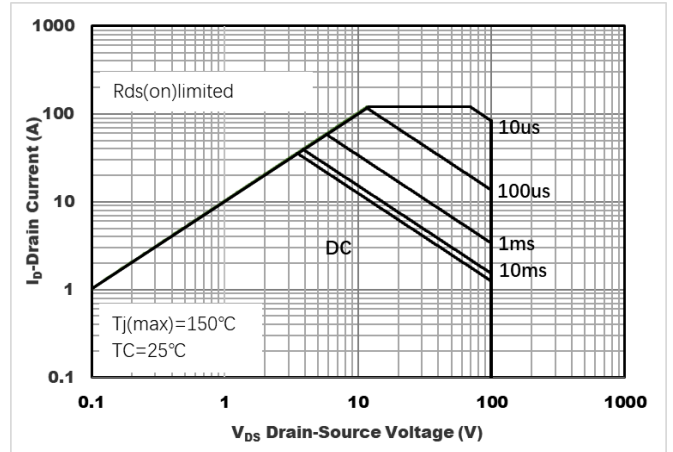


Figure8.Safe Operation Area

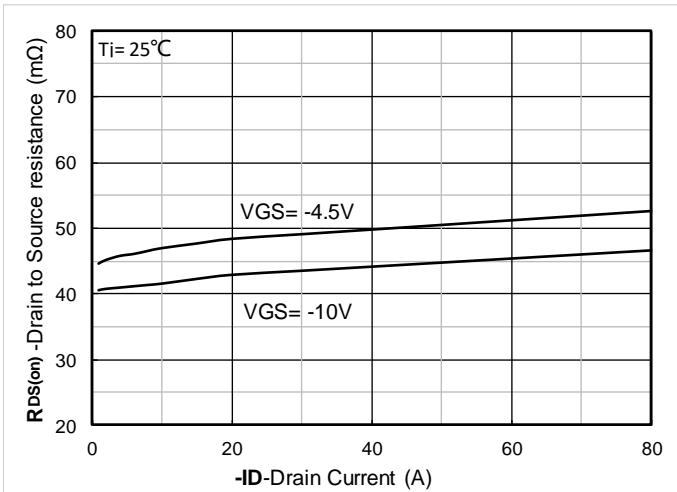


Figure9. RDS(on) VS Drain Current

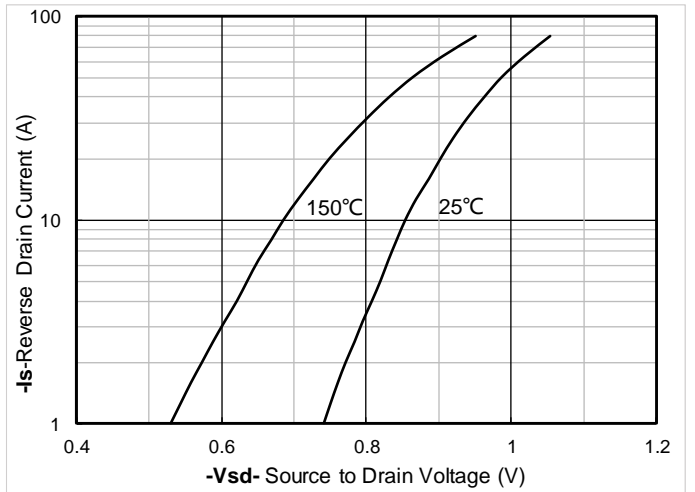


Figure 10. Forward characteristics of reverse diode

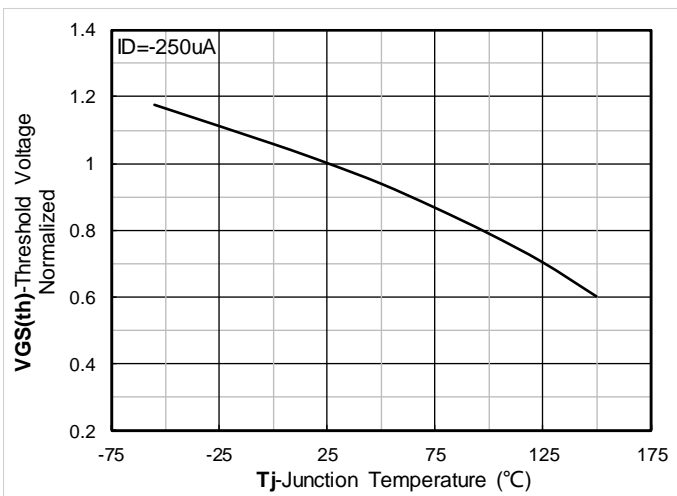


Figure 11. Normalized Threshold voltage

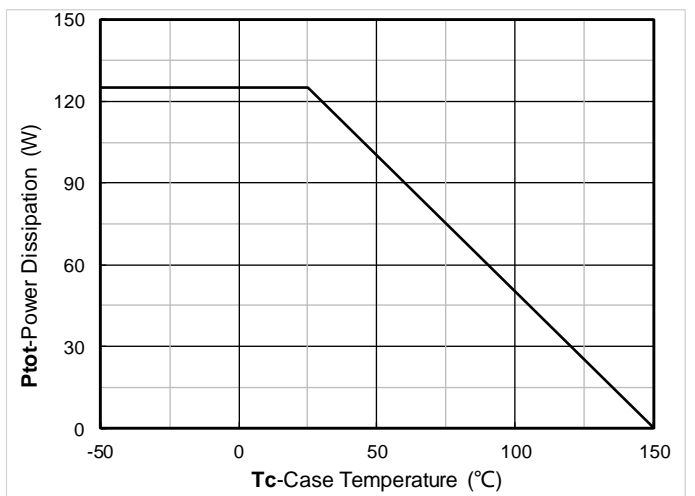


Figure 12. Power dissipation



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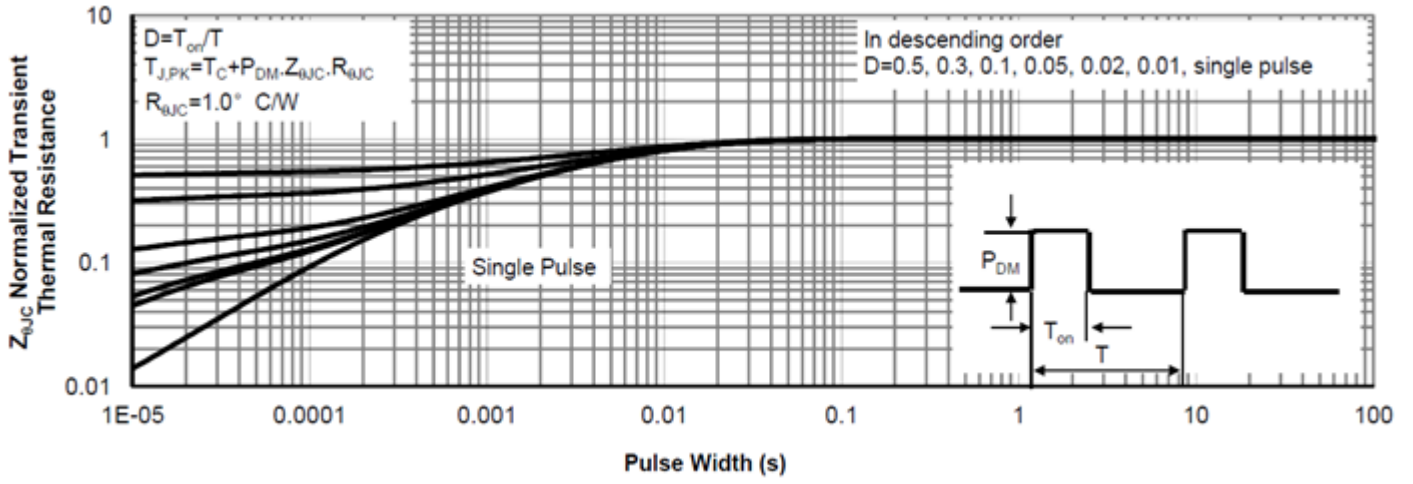
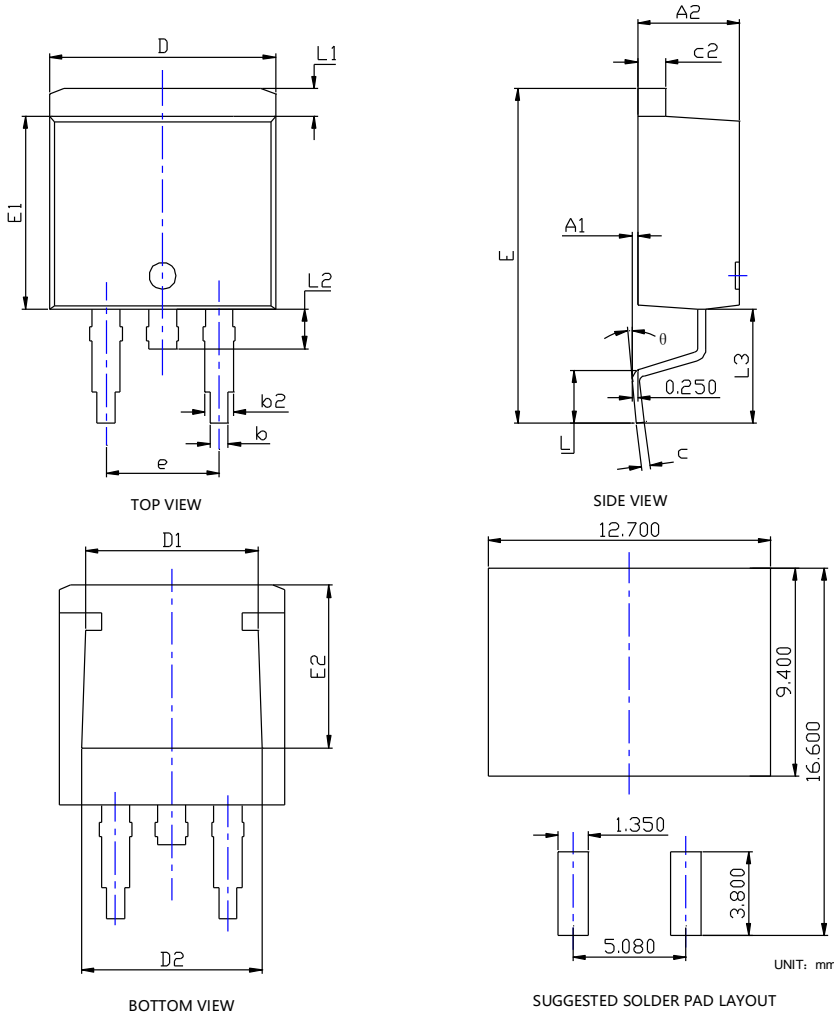


Figure13.Normalized Maximum Transient thermal impedance



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## ■ TO-263-HY Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A1	0.000	---	0.010	0.000	---	0.250
A2	0.174	0.180	0.186	4.430	4.580	4.730
b	0.028	0.032	0.036	0.720	0.820	0.920
b2	0.046	0.050	0.054	1.180	1.280	1.380
c	0.013	0.015	0.018	0.330	0.390	0.450
c2	0.048	0.050	0.053	1.220	1.280	1.340
D	0.394	0.400	0.406	10.000	10.150	10.300
D1	0.295	0.307	0.319	7.500	7.800	8.100
D2	0.303	0.315	0.327	7.700	8.000	8.300
E	0.571	0.591	0.610	14.500	15.000	15.500
E1	0.337	0.341	0.348	8.550	8.700	8.850
E2	0.276	0.287	0.299	7.000	7.300	7.600
e	0.200BSC			5.080BSC		
L	0.070	---	0.110	1.790	---	2.790
L1	0.044	---	0.056	1.120	---	1.420
L2	0.030	---	0.070	0.770	---	1.770
L3	0.197REF			5.000REF		
θ	0°	---	8°	0°	---	8°

NOTE:  
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.  
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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