

N-Channel and P-Channel Complementary MOSFET

Product Summary

NMOS

• V_{DS}	100V
• I_D	1A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	<270m Ω
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<344m Ω

PMOS

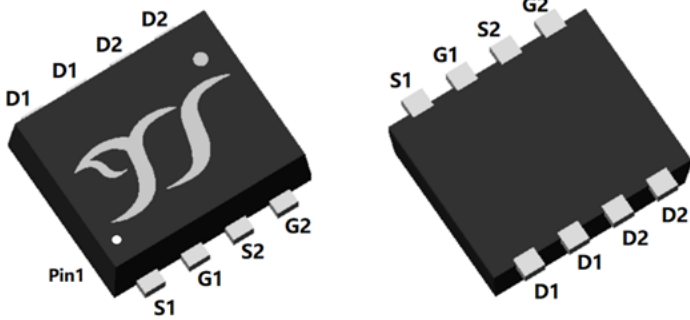
• V_{DS}	-100V
• I_D	-0.9A
• $R_{DS(ON)}$ (at $V_{GS}=-10V$)	<565m Ω
• $R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	<640m Ω

General Description

- Voltage controlled small signal switch
- Fast Switching Speed
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

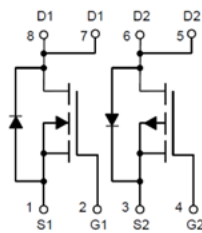
Applications

- Power Management Functions
- Motor Control
- DC-DC convertor



Top View

Bottom View



PDFN3030-8L

Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	NMOS	PMOS	Unit
Drain-source Voltage			V_{DS}	100	-100	V
Gate-source Voltage			V_{GS}	± 20	± 20	V
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^\circ\text{C}$	I_D	1	-0.9	A
		$T_A=100^\circ\text{C}$		0.63	-0.57	
Pulsed Drain Current	$T_C=25^\circ\text{C}$, $t_p=100\mu\text{s}$		I_{DM}	8	-7	A
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^\circ\text{C}$	P_D	1.19	1.13	W
		$T_A=100^\circ\text{C}$		0.47	0.45	
Junction and Storage Temperature Range			T_J, T_{STG}	-55~+150	-55~+150	$^\circ\text{C}$

Thermal resistance

Parameter	Symbol	NMOS		PMOS		Units	
		Typ	Max	Typ	Max		
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	85	105	90	110	$^\circ\text{C/W}$

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJUA320NP10AJ	F1	Q320NP10A	3000	30000	120000	7" reel



YJUA320NP10AJ

■ NMOS Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
		V _{DS} =100V, V _{GS} =0V, T _J =150°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.3	1.8	2.3	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =1A	-	200	270	mΩ
		V _{GS} =4.5V, I _D =1A	-	215	344	
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	1.7	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	1	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	330	-	pF
Output Capacitance	C _{oss}		-	12.5	-	
Reverse Transfer Capacitance	C _{rss}		-	10.8	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =2A	-	8.7	-	nC
Gate-Source Charge	Q _{gs}		-	0.5	-	
Gate-Drain Charge	Q _{gd}		-	0.87	-	
Reverse Recovery Charge	Q _{rr}	I _F =2A, di/dt=100A/us	-	21.7	-	nC
Reverse Recovery Time	t _{rr}		-	20.5	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =2A R _{GEN} =2.7Ω	-	5.5	-	ns
Turn-on Rise Time	t _r		-	3	-	
Turn-off Delay Time	t _{D(off)}		-	15.7	-	
Turn-off fall Time	t _f		-	3.1	-	



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■ PMOS Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-100V, V _{GS} =0V	-	-	-1	μA
		V _{DS} =-100V, V _{GS} =0V, T _J =150°C	-	-	-100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-1.2	-1.7	-2.2	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-0.5A	-	435	565	mΩ
		V _{GS} =-4.5V, I _D =-0.5A	-	475	640	
Diode Forward Voltage	V _{SD}	I _S =-0.5A, V _{GS} =0V	-	-	-1.2	V
Gate resistance	R _G	f=1MHz	-	22	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	-0.9	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-50V, V _{GS} =0V, f=1MHz	-	486	-	pF
Output Capacitance	C _{oss}		-	13.3	-	
Reverse Transfer Capacitance	C _{rss}		-	10.7	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-50V, I _D =-0.5A	-	10.5	-	nC
Gate-Source Charge	Q _{gs}		-	0.74	-	
Gate-Drain Charge	Q _{gd}		-	1.33	-	
Reverse Recovery Charge	Q _{rr}	I _F =-0.5A, di/dt=100A/us	-	18.3	-	nC
Reverse Recovery Time	t _{rr}		-	18.2	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-50V, I _D =-0.5A R _{GEN} =2.7Ω	-	5.2	-	ns
Turn-on Rise Time	t _r		-	25	-	
Turn-off Delay Time	t _{D(off)}		-	50	-	
Turn-off fall Time	t _f		-	132	-	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of R_{θJA} is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with TA =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



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■ NMOS Typical Electrical and Thermal Characteristics Diagrams

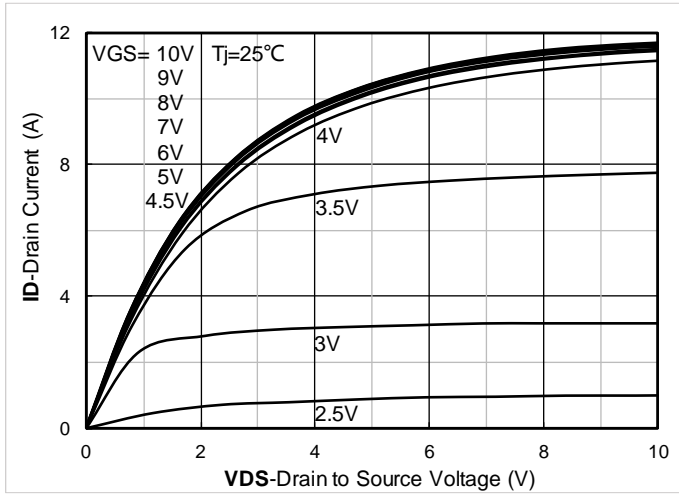


Figure 1. Output Characteristics

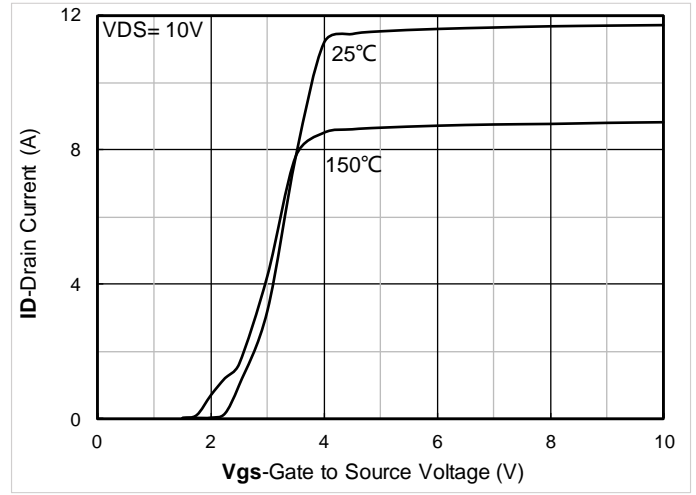


Figure 2. Transfer Characteristics

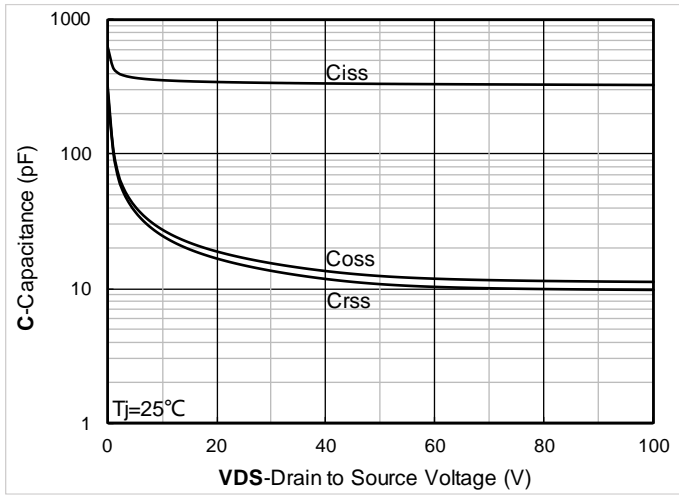


Figure 3. Capacitance Characteristics

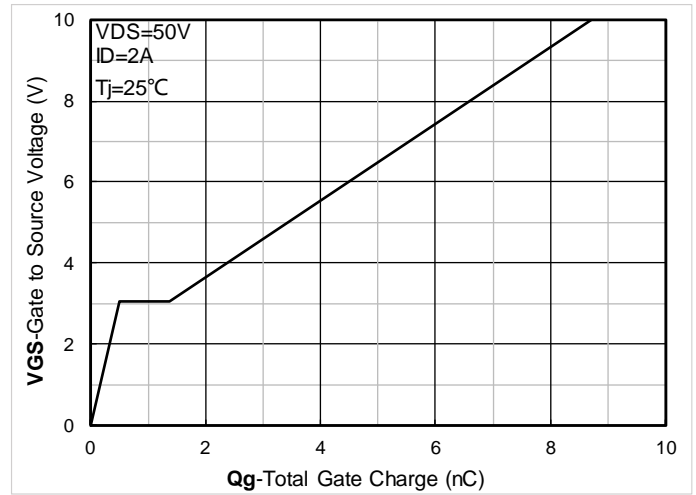


Figure 4. Gate Charge

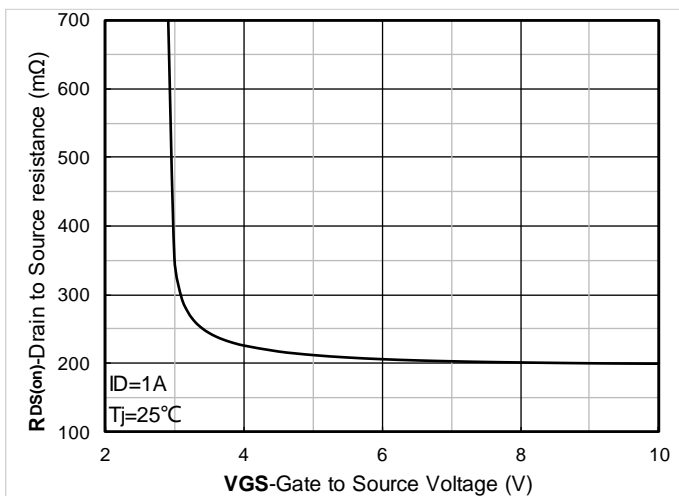


Figure 5. On-Resistance vs Gate to Source Voltage

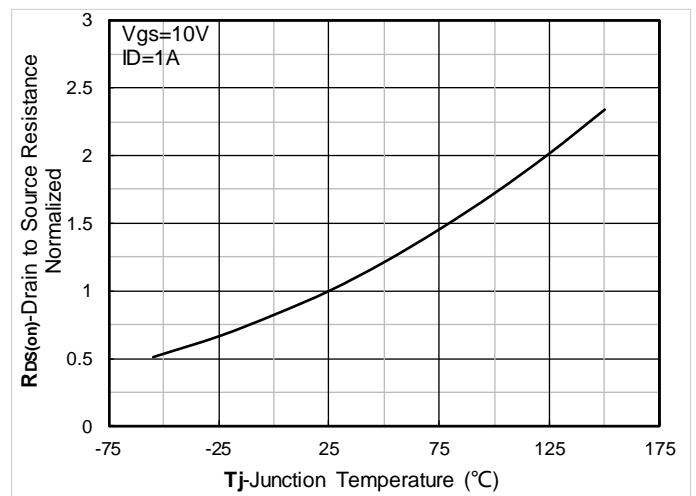


Figure 6. Normalized On-Resistance vs Junction Temperature



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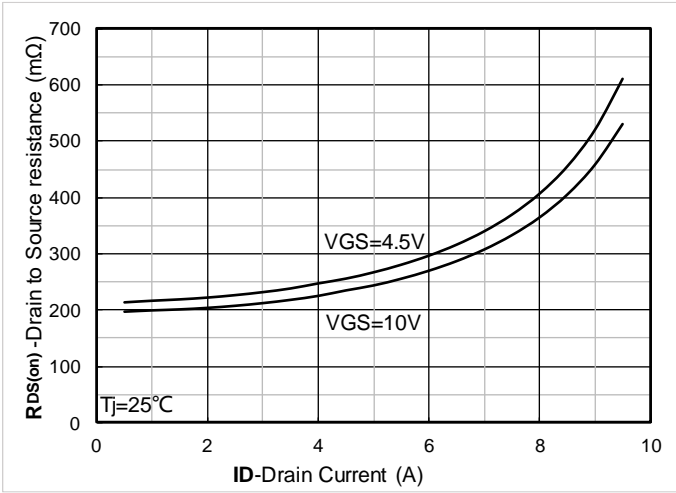


Figure 7. RDS(on) VS Drain Current

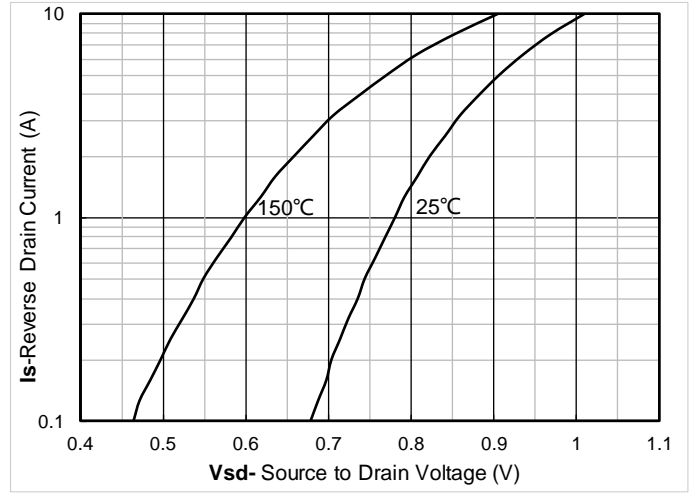


Figure 8. Forward characteristics of reverse diode

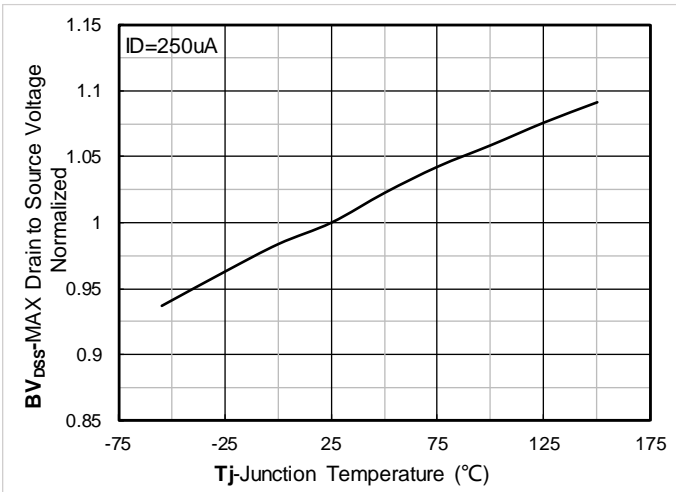


Figure 9. Normalized breakdown voltage

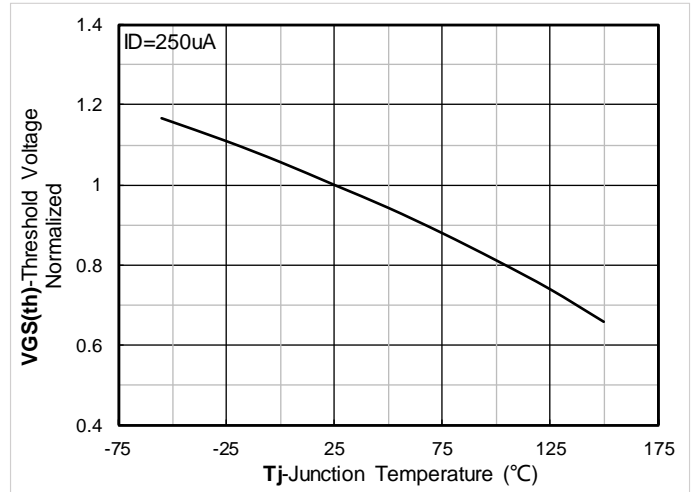


Figure 10. Normalized Threshold voltage

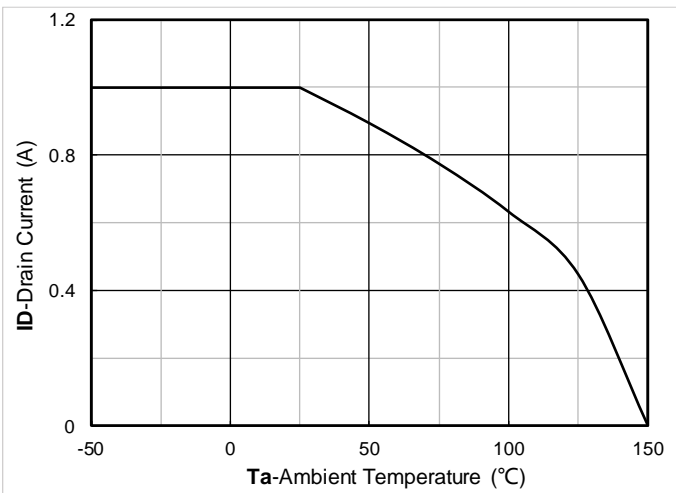


Figure 11. Current dissipation

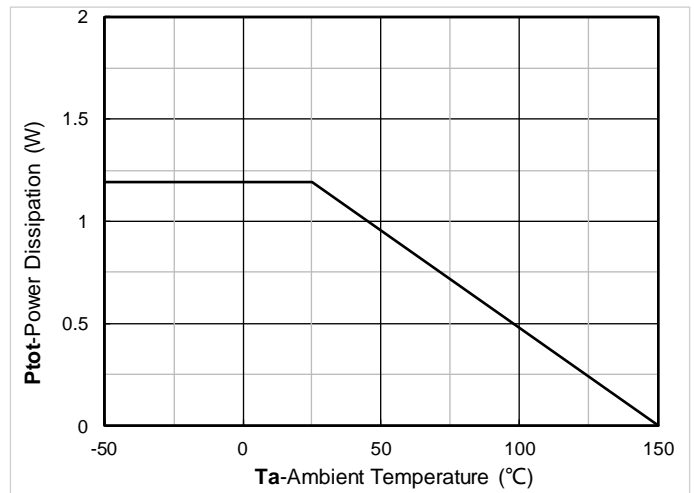


Figure 12. Power dissipation

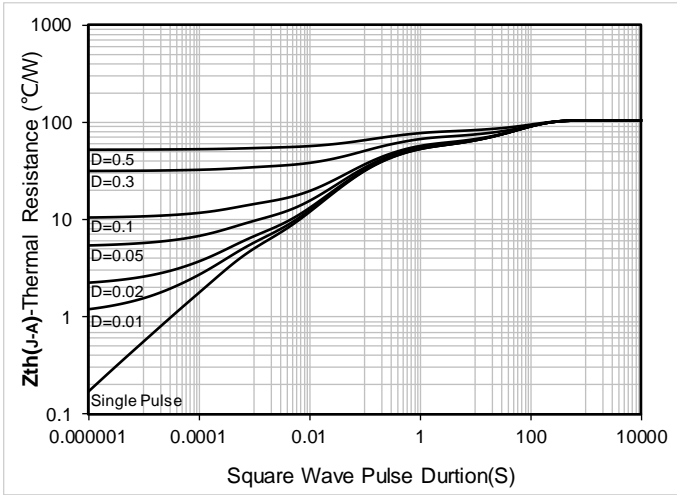


Figure 13. Maximum Transient Thermal Impedance

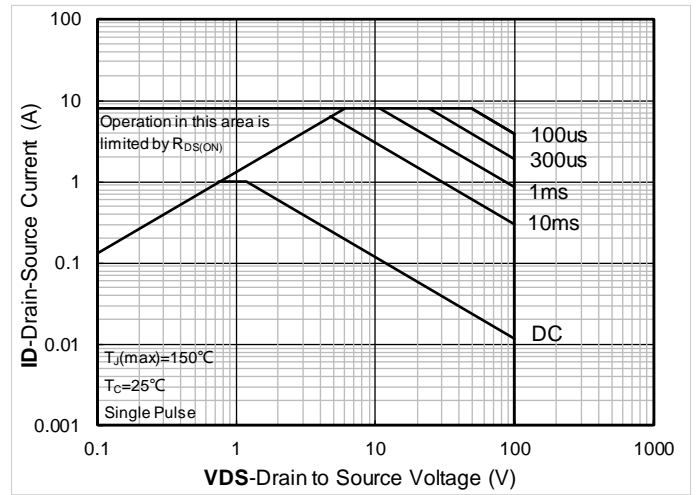


Figure 14. Safe Operation Area

■ PMOS Typical Electrical and Thermal Characteristics Diagrams

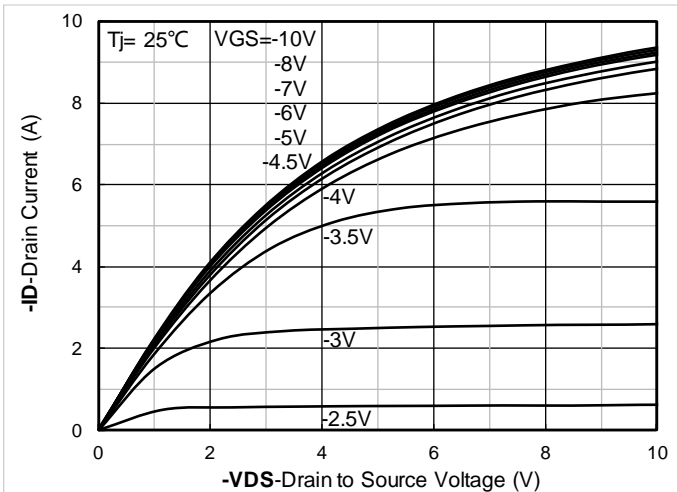


Figure 1. Output Characteristics

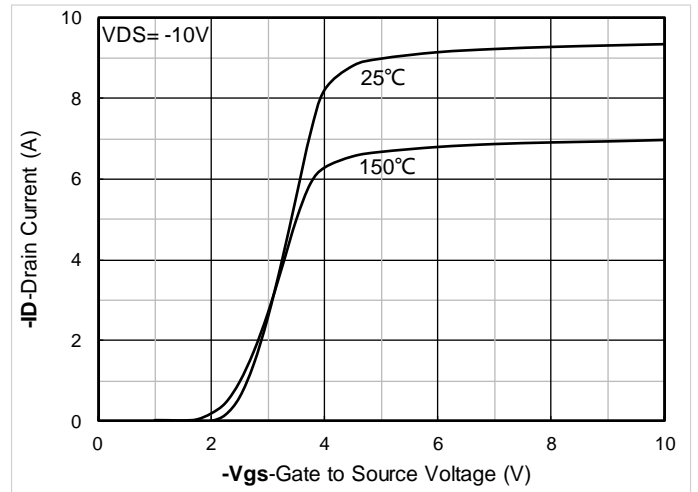


Figure 2. Transfer Characteristics

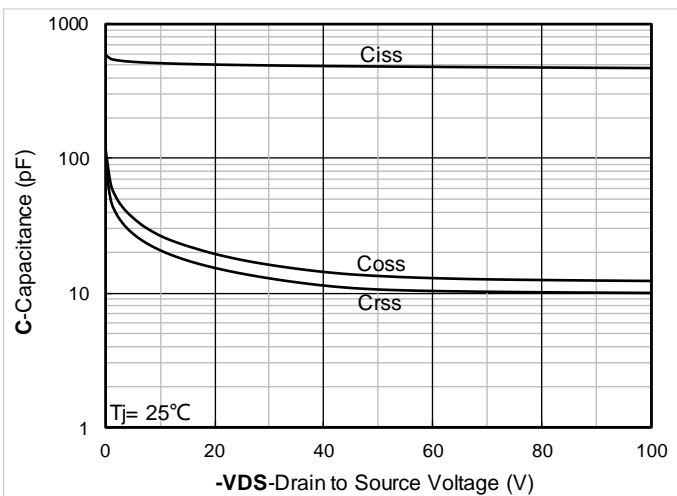


Figure 3. Capacitance Characteristics

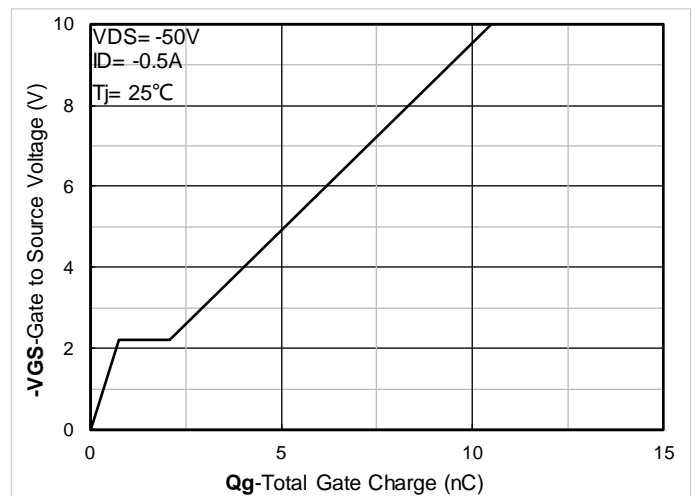


Figure 4. Gate Charge



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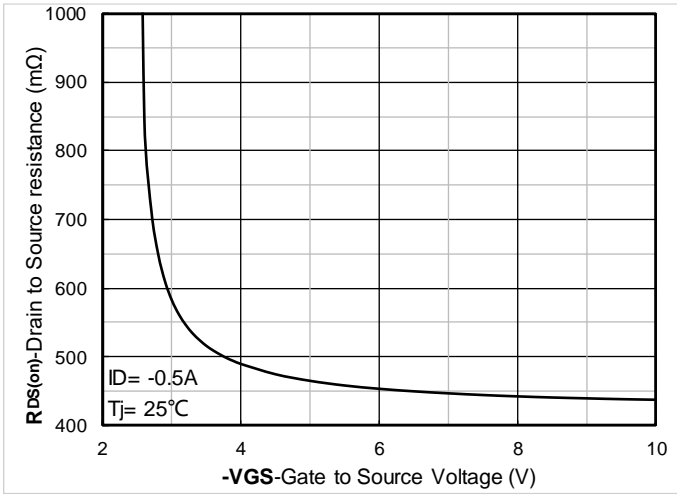


Figure 5. On-Resistance vs Gate to Source Voltage

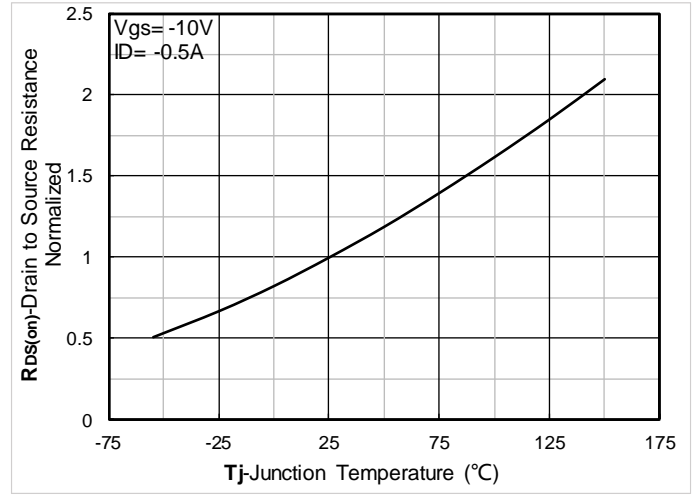


Figure 6. Normalized On-Resistance

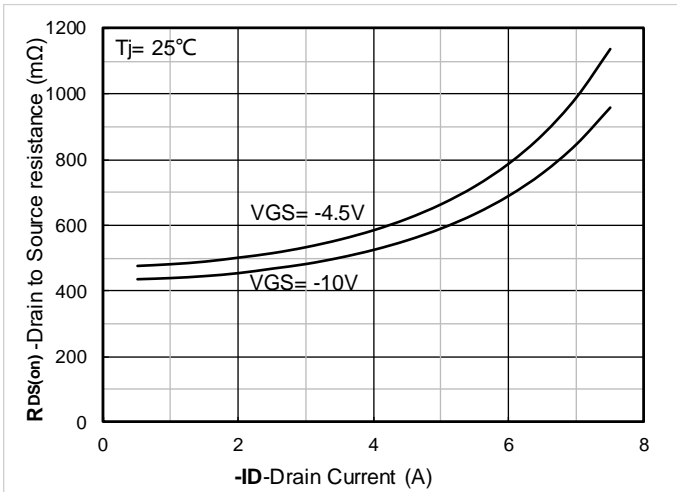


Figure 7. RDS(on) VS Drain Current

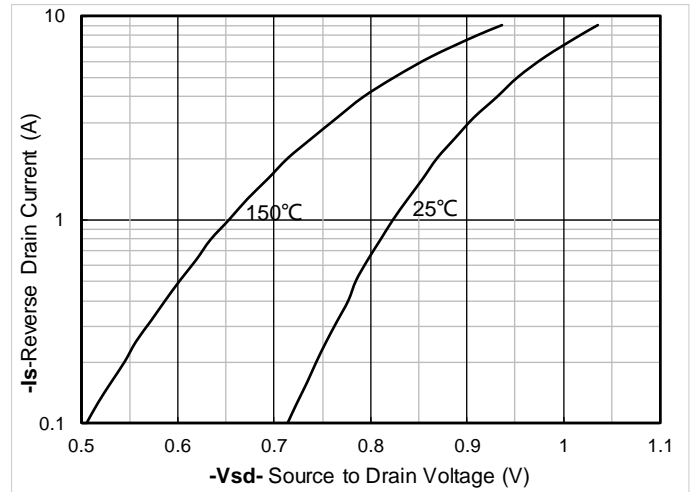


Figure 8. Forward characteristics of reverse diode

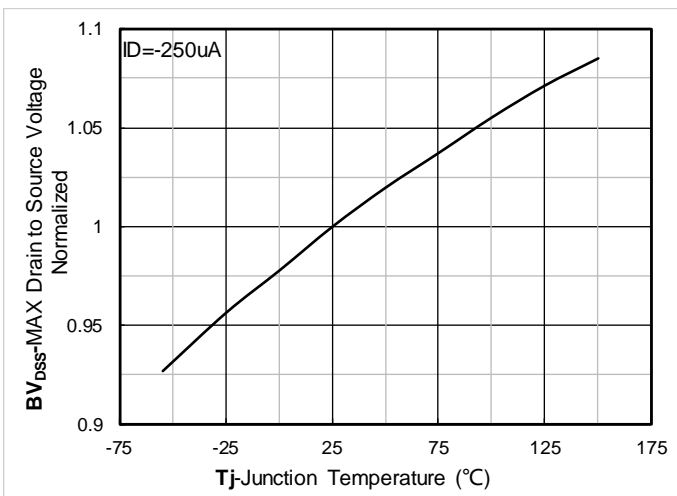


Figure 9. Normalized breakdown voltage

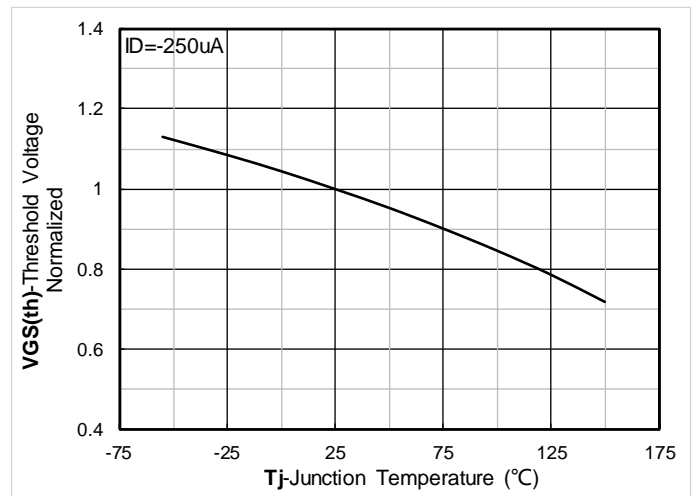


Figure 10. Normalized Threshold voltage



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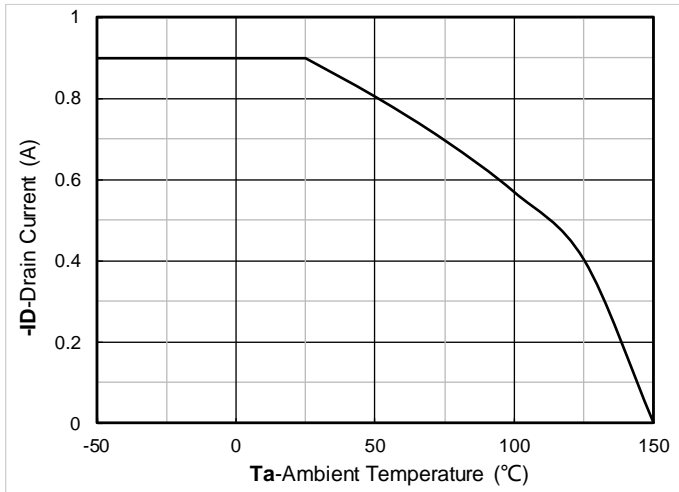


Figure 11. Current dissipation

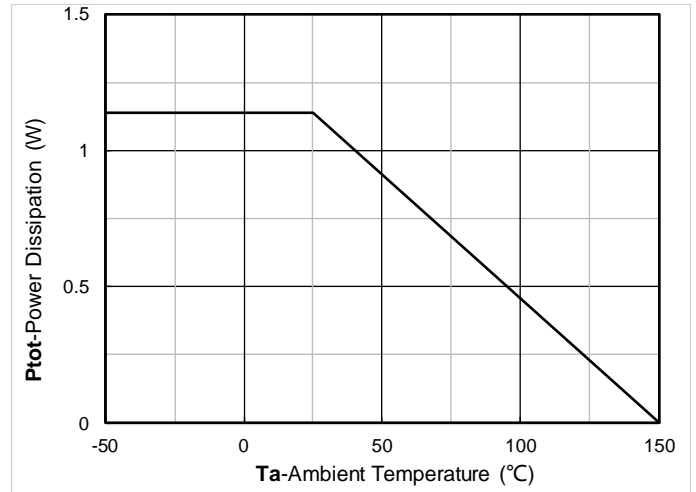


Figure 12. Power dissipation

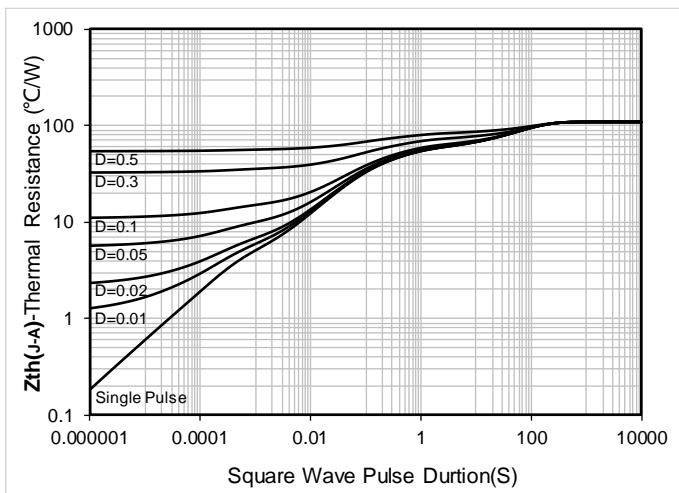


Figure 13. Maximum Transient Thermal Impedance

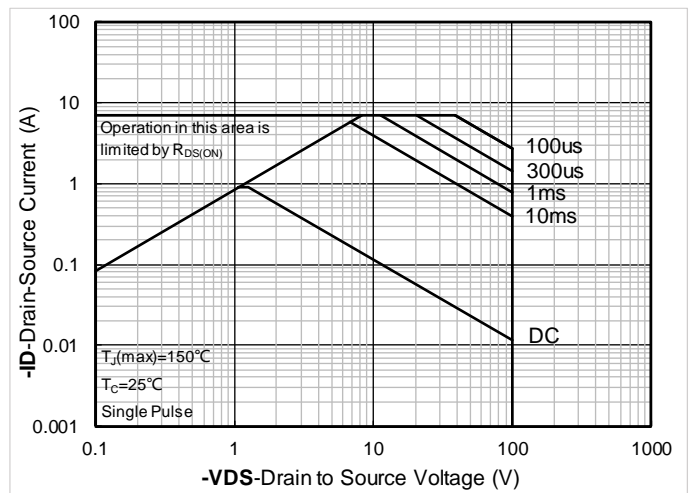
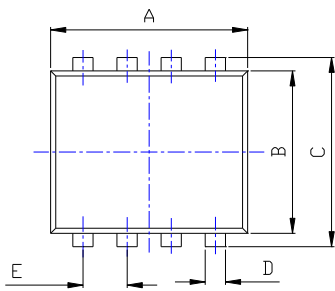


Figure 14. Safe Operation Area

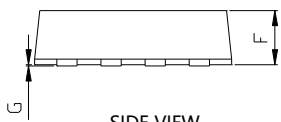


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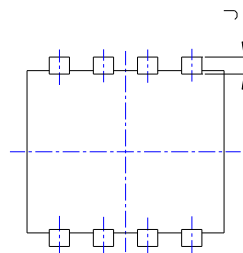
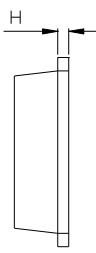
■ PDFN3030-8L Package information



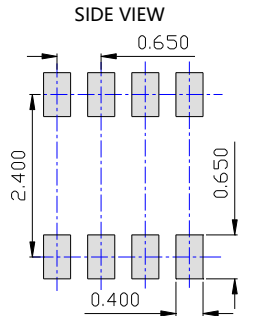
TOP VIEW



SIDE VIEW



BOTTOM VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.108	0.120	2.750	3.050
B	0.089	0.100	2.250	2.550
C	0.104	0.116	2.650	2.950
D	0.008	0.016	0.200	0.400
E	0.026TYP		0.650TYP	
F	0.028	0.035	0.700	0.900
G	0.000	0.004	0.000	0.100
H	0.004	0.012	0.100	0.300
J	0.007	0.015	0.190	0.390

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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